AMENDMENTS

IN THE CLAIMS:

Claims 1-24 (canceled)

25. (Currently Amended) A method for forming EEPROM cell on a substrate having an outer surface, the method comprising the steps of:

forming a deep conductive region of a first conductivity type in the substrate below the substrate's outer surface;

forming first and second conductive regions of a first conductivity type in the substrate below the substrate's outer surface, the first and second conductive regions are laterally displaced from one another by a predetermined distance;

forming an insulating layer outwardly from the outer surface of the substrate, the insulating layer positioned so that its edges are substantially in alignment between the first and second conductive regions;

forming a floating gate layer outwardly from the insulating layer and in substantially the same shape as the insulating layer; and

wherein the deep conductive region is operable to provide a source of charge for placement on the floating gate layer when programming the EEPROM cell and the deep conductive region is formed to a depth substantially below only portions of the first and second conductive regions.

26. (Original) The method of Claim 25 wherein the insulating layer is formed from oxide.

27. (Original) The method of Claim 25 wherein the floating gate layer is formed from polysilicon.

28. (Original) The method of Claim 25 wherein the deep conductive region is doped N+ on the order of 1×10^{16} cm^{-3}.